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July 29, 2003

Commissioner for Patents
Alexandria, VA 22313

RE: Application No. 09/196,185
Filed: November 20, 1998
WIRE FOR LIQUID CRYSTAL DIAPLAYS, LIQUID CRYSTAL DISPLAYS HAVING THE SAME, AND MANUFACTURING METHODS THEREOF
Inventor: Myung-Koo HUR, *et al.*
Our Ref: 6192.0052.AA

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. A Transmittal Letter;

2. A Submission of Verified English Language Translation of Priority Document; and

3. Two Acknowledgement postcards.

It is respectfully requested that the attached copy of the postcard be stamped with the filing date of these documents and returned to our courier.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 23-1951 referencing docket number 6192.0052.AA.

Respectfully submitted,

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Enclosures

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of	Docket No.: 6192.0052.AA
Myung-Koo HUR, *et al.*	
Serial No.: 09/196,185	Group Art Unit: 2871
Confirmation No.: 8847	
Filed: November 20, 1998	Examiner: QI, Zhi Qiang

For: **WIRE FOR LIQUID CRYSTAL DISPLAYS, LIQUID CRYSTAL DISPLAYS HAVING THE SAME, AND MANUFACTURING METHODS THEREOF**

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SUBMISSION OF VERIFIED ENGLISH LANGUAGE TRANSLATION OF PRIORITY DOCUMENT

Sir:

Applicant herewith submits a Verified English language translation of the Certified Copy of the Priority Document of Korean Patent Application no. 97-61315 filed on November 20, 1999.

Please charge any deficiencies in fees and credit any overpayments to Attorney's deposit account no. 23-1951 (McGuireWoods LLP).

Respectfully submitted,

Hae-Chan Park
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Date: July 29, 2003

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I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 97-61315 filed on November 20,1999.

This 24th day of July 24, 2003

Translator: Jo Soung Mook

Jo, Soung-Mook

ABSTRACT OF THE DISCLOSURE

A wire for a liquid crystal display has a dual-layered structure comprising a first layer made of molybdenum or molybdenum alloy, and a second layer made of molybdenum nitride or molybdenum alloy nitride. To manufacture the wire, a layer made of either molybdenum or a molybdenum alloy, and another layer one of either a molybdenum nitride or molybdenum alloy nitride by using reactive sputtering method are deposited in sequence, and then patterned simultaneously. The target for reactive sputtering is made of either molybdenum or molybdenum alloy, and the molybdenum alloy comprises one selected from the group consisting of tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm % of. The reactive gas mixture for reactive sputtering includes an argon gas and inflow amount of the nitrogen gas is at least 50% of argon gas, to minimize the etch rate of the molybdenum nitride layer or the molybdenum alloy nitride layer for ITO etchant.

TITLE OF THE INVENTION

WIRES FOR LIQUID CRYSTAL DISPLAYS, AND MANUFACTURING METHODS THEREOF

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a layout view of a thin film transistor (TFT) array panel according to an embodiment of the present invention.

Figs. 2 and 3 show sectional views of the TFT array panel taken along the lines II-II' and III-III' in Fig. 1, respectively.

Figs. 4A-4F are sectional views of the intermediate structures of a manufacturing method of the TFT array panel shown in Fig. 1 to Fig. 3 according the embodiment of the present invention.

Fig. 5 is a graph illustrating etch rate of a molybdenum-tungsten alloy nitride layer according to the volume of nitrogen gas as a reactive gas for aluminum and ITO etchants.

BACKGRAND OF THE INVENTION

(1) Field of the invention

The present invention relates to wires for liquid crystal displays (LCDs) having high chemical durability and manufacturing methods thereof.

(2) Description of the Related Art

In general, an LCD has a gate wire on a substrate, and the gate wire includes gate lines, gate pads and gate electrodes which transmits scanning signals. The gate wire is covered with a gate insulating layer, and a semiconductor layer is formed on portions of the gate insulating layer opposite the gate electrodes. The LCD also has a data wire on the gate insulating layer,

and the data wire includes data lines, data pads and source electrodes transmitting image signals and drain electrodes connected to the source electrodes through the semiconductor layer. A passivation layer having a contact hole exposing the drain electrode is formed on the data wire, and pixel electrodes which are formed of a transparent conductive material such as ITO (indium tin oxide) and connected to the drain electrodes through the contact hole are formed thereon.

To manufacture the liquid crystal display, deposition, photolithography, and etch steps are required for the gate wire, the data wire, the gate insulating layer, the passivation layer, and the pixel electrodes.

There are two general methods for depositing a thin film, a chemical vapor deposition (CVD) and a physical deposition. The CVD forms the film by the reaction of vapor phase chemicals that contain the required constituents, while a sputtering which is a kind of physical deposition obtains the film by having energetic particles to strike target to be sputtered physically. The CVD is generally used to form the semiconductor layer and insulating layers such as the gate insulating layer and the passivation layer, and the sputtering is used to form metal layers for the gate wire and the data wire and an ITO layer for the pixel electrodes.

The etch method is divided into two types, wet etch using etchants and dry etch using etching gases.

In particular, when an ITO layer is etched by using an etchant, hydrochloric acid and nitric acid are used. However, it may happen that the etchant penetrates the passivation layer, contacts the data wire and the gate

pad, and then erode the data wire and the gate pad. Accordingly, the data wire and the gate pad may be disconnected and/or eroded.

SUMMARY OF THE INVENTION

In view of the above, it is an object of the present invention to provide a data wire having highly chemical endurance against an etchant for a pixel electrode.

A wire according to the present invention is made of either molybdenum nitride layer or molybdenum alloy nitride layer.

The manufacturing method of the wires according to the present invention uses a reactive sputtering method, and the target for the reactive sputtering may be made of a molybdenum alloy including one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %. The reactive gas mixture used for the reactive sputtering may include argon gas and nitrogen gas, and the inflow amount of the nitrogen gas is at least 50% of that of the argon gas.

Because the wires according to the present invention have low etch rate for the ITO etchant including strong acid, the disconnections of the wires are reduced.

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to

those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Fig. 1 shows a layout view of a TFT array panel according to an embodiment of the present invention, and Figs. 2 and 3 show sectional views taken along the lines II-II' and III-III' in Fig. 1, respectively.

The structure of the TFT array panel according to an embodiment of the present invention includes a supplementary wire having highly chemical endurance to prevent disconnections of signal lines.

A gate wire made of either molybdenum or molybdenum alloy is formed on an insulating substrate 100, and the gate wire has a thickness of 1,000 - 4,000 Å and includes a transverse gate line 200, a gate electrode 210, which is a branch of the gate line 200, and a gate pad 230 which is connected to one end of the gate line 200. A supplementary gate wire 250 having a thickness of 300 - 1,000 Å is formed under the gate wire 200, 210 and 230 and made of either molybdenum nitride (MoN_X) or molybdenum alloy nitride (Mo-alloy-N_X). The supplementary gate wire 250 may be located on the gate wire 200, 210 and 230. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium and nickel of the content of 0.1 to less than 20 atm %.

A gate insulating layer 300 covers the gate wire 200, 210 and 230, a hydrogenated amorphous silicon (a-si:H) layer 400 and a doped hydrogenated amorphous silicon layer 410 and 420 including N type impurity are sequentially formed on the gate insulating layer 300 opposite the gate electrode 210, and the portions 410 and 420 of the doped amorphous silicon layer are opposite each other with respect the gate electrode 220.

A data line 500 in the longitudinal direction is formed on the gate insulating layer 300, a source electrode 510 which is a branch of the data line 500 is formed on the one portion 410 of the doped amorphous silicon layer, and a drain electrode 520 opposite the source electrode 510 with respect to the gate electrode 210 is formed on the other portion 420 of the doped amorphous silicon layer. Here, the data wire including the data line 500, the source and drain electrodes 510 and 520 is made of either molybdenum or molybdenum alloy.

A supplementary data wire 550 made of either molybdenum nitride or molybdenum alloy nitride is formed under the data wire 500, 510 and 530. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium, and nickel of the content of 0.1 to less than 20 atm %. The supplementary data wire 550 may be located on the data line 500.

A passivation layer 600 is formed on the data wire 500, 510 and 520 and portions of the amorphous silicon layer 400 which is not covered by the data wire 500, 510 and 520. The passivation layer 600 has a contact hole C1 exposing the drain electrode 520, and another contact hole C2 exposing the gate pad 230 along with the gate insulating layer 300. Here, the description of

a data pad connected to the data line 500 is omitted.

A pixel electrode 700 formed of ITO (indium tin oxide) and connected to the drain electrode 520 through a contact hole C1 is formed on the passivation layer 600. Furthermore, a gate ITO layer 710 connected to the gate pad 230 through the contact hole C2 and improving the contact characteristic is formed on the passivation layer 700.

A manufacturing method of the TFT array panel having molybdenum nitride layer or molybdenum alloy nitride layer as a supplementary wire to prevent the disconnection of the wire during ITO etches process will now be described.

Figs. 4A-4D show cross sectional views of the intermediate structures of a manufacturing method of the TFT array panel according to the embodiment of the present invention, and taken along the lines II-II' and III-III' in Fig. 1, respectively.

As shown in Fig. 4A, a nitride layer 251 made of either molybdenum nitride or molybdenum alloy nitride is deposited on a transparent insulating substrate 100 by using reactive sputtering method to form a supplementary gate wire. The target for the reactive sputtering is made of either molybdenum and molybdenum alloy having one selected from tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm %. A reactive gas mixture includes argon gas (Ar) and nitrogen gas (N_2), and the inflow amount of the nitrogen gas is equal to or more than 0.5 times that of argon gas. Thereafter, a metal layer 201 made of either molybdenum or molybdenum alloy is deposited by sputtering. The metal layer 201 may be

deposited before the deposition of the nitride layer 251.

As shown in Fig. 4B, the metal layer 201 and the nitride layer 251 are sequentially patterned to form a gate wire including a gate line 200, a gate electrode 210 and a gate pad 230, and a supplementary gate wire 250 by performing a wet etch using an etchant such as aluminum etchant comprising nitric acid, acetic acid, phosphoric acid and dionized water.

As shown in Fig. 4C, a gate insulating layer 300 made from silicon nitride, a hydrogenated amorphous silicon layer and an extrinsic or doped hydrogenated amorphous silicon layer highly doped with N type impurity are sequentially deposited by plasma-enhanced chemical vapor deposition (PECVD hereafter). The amorphous silicon layer and the extrinsic amorphous silicon layer are patterned by photolithography to form an active pattern 401 and 411. A nitride layer 551 made of either molybdenum nitride or molybdenum alloy nitride with the thickness of 300~1,000 Å is deposited by using reactive sputtering method, and a metal layer 501 made of either molybdenum or molybdenum alloy with the thickness of 1,000 - 4,000 Å is deposited. The metal layer 501 may be deposited before the deposition of the nitride layer 551 When the thickness of the nitride layer 551 is less than 300 Å, it is difficult to obtain the uniform thickness, and the thickness of more than 1,000 Å is deteriorates the following etch step.

As shown in Fig. 4D, the metal layer 501 and the nitride layer 551 are sequentially patterned to form a data wire including a data line 500, a source electrode 510, a drain electrode 520 and a data pad (not shown), and a

supplementary wire 550 by performing wet-etch using the above-described aluminum etchant. Because the etch rate for the upper metal layer 501 is larger than the etch rate for the low nitride layer 551, the metal layer 501 may be over-etched. Accordingly, it is desirable that the thickness of the nitride layer 551 is less than 1,000 Å to prevent the over-etch of the metal layer 501.

Thereafter, exposed portions of the extrinsic amorphous silicon layer 411 is removed such that the extrinsic amorphous silicon layer is then divided two portions 410 and 420, and the central portion of the amorphous silicon layer 400 is exposed.

As shown in Fig. 4E, a passivation layer 600 is deposited and patterned along with the gate insulating layer 300 to form contact holes C1 and C2 exposing the drain electrode 520 and the gate pad 230, respectively.

Finally, an ITO layer is deposited and patterned to form a pixel electrode 700 connected to the drain electrode 520 through the contact hole C1, a gate ITO layer 710 connected to the gate pad 230 through the contact hole C2, and a data ITO layer, as shown in Fig. 4F. Here, the etchant for the ITO layer comprises hydrochloric acid and nitric acid, which may penetrate along the crack of the passivation layer 600 or along the edges of the ITO wire 700 and 710, and then may disconnect and/or erode reach the data wire 500, 510 and 520, and the gate pad 230.

However, because the supplementary gate wire 250 and the supplementary data wire 550 have a low chemical reactivation against the ITO etchant, the gate wire 200, 210 and 230, and the data wire 500, 510 and 520 through the supplementary gate wire 250 and the supplementary data wire 550

are not disconnected.

Next, the etch rate of a molybdenum-tungsten alloy nitride layer as function of volume of nitrogen gas as a reactive gas for aluminum and ITO etchants is described to confirm the low chemical reactivation of the supplementary gate and data wires 250 and 550 for aluminum and ITO etchants.

Fig. 5 is a graph illustrating etch rate of a molybdenum-tungsten alloy nitride layer as function of inflow amount of nitrogen gas as a reactive gas for aluminum and ITO etchants. The horizontal axis indicates the inflow amount of a nitrogen gas in sccm, and the vertical axis indicates etch rates of a molybdenum-tungsten alloy nitride layer in Å/sec for an aluminum etchant and an ITO etchants. In this experiment, the inflow amount 105 sccm of the Ar gas is fixed, and that of nitrogen gas varies from zero to 160 sccm during reactive sputtering. The etch rate of the molybdenum-tungsten alloy nitride layer for the aluminum etchant and the ITO etchant decreases as the inflow amount of nitrogen gas with respect to argon gas increases. Its etch rates for the aluminum etchant and the ITO etchant are respectively 95 Å/sec and 35 Å/sec when inflow amount of argon gas is 105 sccm and that of nitrogen gas is 50 sccm. The etch rate below 35 Å/sec implies that the etched thickness is negligible. In addition, because the mount of the ITO etchant penetrating along the narrow crack having a width of less than 100 μm of the passivation layer is very small, the etched thickness of below 35 Å/sec is ignorable. In the meantime, the etch rate depends on the ratio of argon gas and nitrogen gas.

For example, when the inflow amount of the nitrogen gas is at least 50 % of that of the argon gas, not only the supplementary gate and data wires 250 and 550 is simultaneously etched with the gate wire 200, 210 and 230, and the data wire 500, 510 and 520, but also the supplementary gate and data wires 250 and 550 is rarely etched for the ITO etchant.

As above described, when the inflow amount of the nitrogen gas is at least 50 % of that of the argon gas during sputtering, the supplementary gate and data wires 250 and 550 may have high chemical endurance against an ITO etchants.

Accordingly, by forming a wire having highly chemical endurance against an ITO etchant, the ITO etchant prevents the wire forming disconnecting and /or eroding in the present invention

In the drawings and specification, there have been disclosed typical preferred embodiments of the present invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

WHAT IS CLAIMED IS:

1. A manufacturing method of a molybdenum-metal alloy nitride layer by a reactive sputtering using argon gas and nitrogen gas as a reactive gas mixture:

wherein a target for the reactive sputtering is made of molybdenum alloy comprising a metal of 0.1 to less than 20 atm %, and inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

2. The method of the claim 1, wherein the metal is one selected from the group consisting of tungsten, chromium, zirconium and nickel.

3. A molybdenum-metal alloy nitride layer manufactured by the method of claim 2.

4. A wire for a display liquid display comprising:

a main layer made of either molybdenum or molybdenum alloy;

a supplementary layer which is located either on or under the main layer and made of either molybdenum nitride or molybdenum alloy nitride.

5. The wire of claim 4, wherein the supplementary layer comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel.

6. A manufacturing method of a wire for a liquid crystal display comprising the steps of:

depositing a first layer made of either molybdenum or molybdenum alloy on a substrate;

depositing a second layer made of either molybdenum nitride or molybdenum alloy nitride by using reactive sputtering; and

patterning simultaneously the second and the first layers.

7. The manufacturing method of claim 6, wherein a target for the reactive sputtering is made of either molybdenum or molybdenum alloy, and

the molybdenum alloy comprises one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %

8. The manufacturing method of claim 7, wherein a reactive gas mixture for the reactive sputtering includes argon gas and nitrogen gas, and the nitrogen gas inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

9. The manufacturing method of claim 8, wherein the thickness of the second layer is 300 to 1,000 Å.

10. The manufacturing method of claim 9, wherein the target of molybdenum alloy comprises chromium.

11. A manufacturing method of a wire for a liquid crystal display comprising the steps of:

depositing a first layer made of either molybdenum nitride or molybdenum alloy nitride by using reactive sputtering;

depositing a second layer made of either molybdenum or molybdenum alloy on a substrate; and

patterning simultaneously the second and the first layers.

12. The manufacturing method of claim 11, wherein a target for the reactive sputtering is made of either molybdenum or molybdenum alloy, and

the molybdenum alloy comprises one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %.

13. The manufacturing method of claim 12, wherein a reactive gas

mixture for the reactive sputtering includes argon gas and nitrogen gas, and the nitrogen gas inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

14. The manufacturing method of claim 13, wherein the thickness of the first layer is 300 to 1,000 Å.

15. The manufacturing method of claim 14, wherein the target of molybdenum alloy comprises chromium.

16. A display liquid display comprising:

an insulating substrate;

a gate wire formed on the substrate;

a gate insulating layer covering the gate wire;

a data wire which is made of one of either molybdenum or molybdenum alloy and formed on the gate insulating layer;

a supplementary data wire which is located either on or under the data wire and made of either molybdenum nitride or molybdenum alloy nitride;

a passivation layer formed on the data wire or the supplementary data wire; and

an ITO pixel electrode formed on the passivation layer and connected to the data wire through contact formed in the passivation layer.

17. The liquid crystal display of claim 14, wherein the supplementary data wire comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel.

18. The liquid crystal display of 17, further comprising:

a supplementary gate wire which is located either on or under the gate

wire and made of either molybdenum nitride or molybdenum alloy nitride.

19. The liquid crystal display of claim 18, wherein the supplementary gate wire comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel.

20. A manufacturing method of a liquid crystal display comprising the steps of:

forming a gate wire on a substrate;

forming a gate insulating layer on the gate wire;

forming a semiconductor layer on the gate insulating layer;

depositing a first layer made of either molybdenum or molybdenum alloy;

depositing a second layer made of either molybdenum nitride or molybdenum alloy nitride by using reactive sputtering method;

patterning simultaneously the second and the first layer to form a data wire and a supplementary data wire;

forming a passivation layer on the data wire or the supplementary data wire; and

forming a pixel electrode made of ITO.

21. The manufacturing method of claim 20, wherein a target for the reactive sputtering is made of either molybdenum or molybdenum alloy, and

the molybdenum alloy comprises one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %.

22. The manufacturing method of claim 21, wherein a reactive gas mixture for the reactive sputtering includes argon gas and nitrogen gas, and the

nitrogen gas inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

23. The manufacturing method of claim 20, wherein the thickness of the second layer is 300 to 1,000 Å.

ABSTRACT OF THE DISCLOSURE

The present invention is to provide a wiring line assembly bearing low resistance and good adhesion characteristics, a thin film transistor array substrate including the wiring line assembly, and a method for manufacturing the same. The wiring line assembly is made of Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements and the alloy elements each bearing a low melting point and a high diffusion coefficient. The thin film transistor array substrate basically includes a gate line assembly based on an Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements and the alloy elements each bearing a low melting point and a high diffusion coefficient. The gate line assembly comprises a gate electrode and a gate line. A data line assembly crosses over the gate line assembly while being insulated from the gate line assembly. The data line assembly comprises a source electrode, a drain electrode and a data line. A semiconductor layer contacts the source electrode and the drain electrode. The semiconductor layer forms a thin film transistor together with the gate electrode, the source electrode and the drain electrode. A pixel electrode is connected to the drain electrode. The data line assembly may include the Ag alloy comprising Ag and at least one of alloy elements and the alloy elements each bearing a low melting point and a high diffusion coefficient.

Representative figure

Figure 7

Index

Line assembly, diffusion coefficient, low melting point, alloy elements, Ag alloy

TITLE OF THE INVENTION

WIRING LINE ASSEMBLY FOR THIN FILM TRANSISTOR ARRAY SUBSTRATE AND A METHOD FOR FABRICATING THE SAME

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a graph illustrating the adhesion test results for Ag, AgAl, AgMg and Cr;

Fig. 2 is a graph illustrating the AES analysis results for a sample of an AgMg-based layer under deposition;

Fig. 3 is a graph illustrating the AES analysis results for a sample of an AgMg-based layer where heat-treatment is made at 400℃ under a vacuum atmosphere;

Fig. 4 is a graph illustrating the AES analysis results for a sample of an AgAl-based layer line under deposition;

Fig. 5 is a graph illustrating the AES analysis results for a sample of an AgAl-based layer where heat-treatment is made at 400℃ under a vacuum atmosphere;

Figs. 6A and 6B illustrate the process of forming an oxide layer on the surface and the interface of an Ag alloy-based layer through heat treatment;

Fig. 7 is a graph illustrating the available range of melting points and diffusion coefficients of the alloy content for Ag alloy;

Fig. 8 is a graph illustrating the available range of melting points and enthalpies of the alloy content for Ag alloy;

Fig. 9 is a plan view of a thin film transistor array substrate according to a first preferred embodiment of the present invention;

Fig. 10 is a cross sectional view of the thin film transistor array substrate taken along the X-X' line of Fig. 9;

Fig. 11A illustrates the first step of fabricating the thin film transistor array substrate shown in Fig. 9;

Fig. 11B is a cross sectional view of the thin film transistor array substrate taken along the XIb-XIb' line of Fig. 11A;

Fig. 12A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 9 following that illustrated in Fig. 11A;

Fig. 12B is a cross sectional view of the thin film transistor array substrate taken along the XIIb-XIIb' line of Fig. 12A;

Fig. 13A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 9 following that illustrated in Fig. 12A;

Fig. 13B is a cross sectional view of the thin film transistor array substrate taken along the XIIIb-XIIIb' line of Fig. 13A;

Fig. 14A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 9 following that illustrated in Fig. 13A;

Fig. 14B is a cross sectional view of the thin film transistor array substrate taken along the XIVb-XIVb' line of Fig. 14A;

Fig. 15A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 9 following that illustrated in Fig. 14A;

Fig. 15B is a cross sectional view of the thin film transistor array substrate taken along the XVb-XVb' line of Fig. 15A;

Fig. 16 is a plan view of a thin film transistor array substrate according to a second preferred embodiment of the present invention;

Fig. 17 is a cross sectional view of the thin film transistor array substrate taken

along the XVII-XVII' line of Fig. 16;

Fig. 18A illustrates the first step of fabricating the thin film transistor array substrate;

Fig. 18B is a cross sectional view of the thin film transistor array substrate taken along the XVIIIb-XVIIIb' line of Fig. 18A;

Fig. 19A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 16 following that illustrated in Fig. 18A;

Fig. 19B is a cross sectional view of the thin film transistor array substrate taken along the XIXb-XIXb' line of Fig. 19A;

Fig. 20A illustrates the step of fabricating the thin film transistor array substrate following that illustrated in Fig. 19A;

Fig. 20B is a cross sectional view of the thin film transistor array substrate taken along the XXb-XXb' line of Fig. 20A;

Fig. 21A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 16 following that illustrated in Fig. 20A;

Fig. 21B is a cross sectional view of the thin film transistor array substrate taken along the XXIb-XXIb' line of Fig. 21A;

Fig. 22A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 16 following that illustrated in Fig. 21A;

Fig. 22B is a cross sectional view of the thin film transistor array substrate taken along the XXIIb-XXIIb' line of Fig. 22A;

Fig. 23A illustrates the step of fabricating the thin film transistor array substrate shown in Fig. 16 following that illustrated in Fig. 22A;

Fig. 23B is a cross sectional view of the thin film transistor array substrate taken along the XXIIIb-XXIIIb' line of Fig. 23A; and

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a wiring line assembly, a thin film transistor substrate, and a method for fabricating the same and, more particularly, to a wiring line assembly used for a liquid crystal display, a thin film transistor substrate, and a method for fabricating the same.

(b) Description of the Related Art

Generally, wiring lines for a semiconductor device or a display device are used for signal transmission, and hence, it becomes important lines to keep such wiring away from signal delays as much as possible.

Particularly, as a large-size high-resolution liquid crystal display develops, it becomes more important that the thin film transistor array substrate for such a liquid crystal display should involve low resistance wiring lines to minimize the signal delay. For instance, a low resistance metal such as Al or Al alloy may be used for the wiring purpose.

However, the Al or Al alloy-based wiring lines bear a weak physical or chemical characteristic. The Al or Al alloy erodes easily at the contacting area, when contacting other conductive materials.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a wiring line assembly bearing low resistance and good adhesion characteristics, a thin film transistor array substrate including the wiring line assembly and a method for manufacturing the same.

This and other objects may be achieved by a thin film transistor array substrate having a wiring line assembly with the following features.

The wiring line assembly is formed with an Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements. Each of the alloy elements bears a low melting point.

Each of the alloy elements each bear a diffusion coefficient of 1.5E-12cm^2/sec or more. The alloy elements each bear a melting point of 1500K or less. The wiring line assembly is formed with an Ag alloy comprising Ag and at least one of alloy elements and the alloy elements each bearing a low melting point. The composition content ratio of the alloy elements to the Ag alloy is 20at% or less. The alloy elements are selected from the group consisting of Li, Mg, Al, Sm, and Mn. The Ag alloy is used for reflection electrodes for a reflection type liquid crystal display.

According to one aspect of the present invention, the thin film transistor array substrate basically includes a gate line assembly based on an Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements and the alloy elements each bear a low melting point. The gate line assembly comprises a gate electrode and a gate line. A data line assembly crosses over the gate line assembly while being insulated from the gate line assembly. The data line assembly comprises a source electrode, a drain electrode and a data line. A semiconductor layer contacts the source electrode and the drain electrode. The semiconductor layer forms a thin film transistor together with the

gate electrode, the source electrode and the drain electrode. A pixel electrode is connected to the drain electrode.

Herein the data line assembly may be based on an Ag alloy. The Ag alloy for the data line assembly comprises Ag and at least one of alloy elements and the alloy elements each bear a low melting point. the alloy elements each bear a diffusion coefficient of 1.5E-12 cm^2/sec or more. The alloy elements each bear a melting point of 1500K or less. The composition content ratio of the alloy elements to the Ag alloy is 10at% or less. The alloy elements may be selected from the group consisting of Li, Mg, Al, Sm, and Mn.

Herein, the thin film transistor array substrate further comprises an insulating substrate under the gate line assembly, a gate insulating layer covering the gate line assembly and being under the semiconductor layer, and a protective layer covering the data line assembly with a contact hole exposing the drain electrode. The drain electrode is placed on the semiconductor layer together with the source electrode and the pixel electrode is connected to the drain electrode through the contact hole..

Herein, the semiconductor layer is formed of hydrogenated amorphous silicon, and the thin film transistor array substrate further comprises an oxide layer formed on the gate line assembly and an alloy element - oxide layer being interposed between the source electrode and the semiconductor layer and between the drain electrode and the semiconductor layer.

And, the thin film transistor array substrate further comprises an insulating substrate under the semiconductor layer having a source region, a drain region and a channel region, a gate insulating layer covering the semiconductor layer and being

under the gate line assembly, an inter-layered insulating layer covering the gate line assembly in which the inter-layered insulating layer and the gate insulating layer have contact holes exposing the source region and the drain region and the source and the drain electrodes are connected to the source and the drain regions through the contact holes, and a protective layer covering the data line assembly with a contact hole exposing the drain electrode in which the pixel electrode is connected to the drain electrode through the contact hole of the protective layer.

The semiconductor layer may be formed with poly-crystalline silicon. The thin film transistor array substrate further comprises an alloy element - oxide layer. The alloy element - oxide layer is interposed between the source electrode and the semiconductor layer and between the drain electrode and the semiconductor layer.

In a method for fabricating the thin film transistor array substrate, a gate line assembly is formed on an insulating substrate with an Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements and the alloy elements each bearing a low melting point. The gate line assembly comprises a gate electrode and a gate line. A gate insulating layer is formed on the substrate such that the gate insulating layer covers the gate line assembly. A semiconductor layer is formed on the gate insulating layer. A data line assembly is formed on the semiconductor layer. The data line assembly comprises a source electrode, a drain electrode and a data line. A protective layer is formed on the substrate such that the protective layer covers the data line assembly. A contact hole exposing the drain electrode is formed in the protective layer. A pixel electrode is formed on the protective layer such that the pixel electrode is connected to the drain electrode through the contact hole.

Herein, the gate line assembly or the data line assembly is formed with an Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements each bearing a low melting point. The line assemblies are formed through depositing an Ag alloy layer onto the substrate through sputtering a target of the Ag alloy with an oxygen concentration of 5000ppm or less. The Ag alloy layer is patterned through a photolithography. The protective layer is formed through heat treatment at 200℃ or more. The alloy element of the Ag alloy layer for the data line assembly reacts with a silicon oxide layer to form an alloy element – oxide layer during the process of heat treatment for forming the protective layer where the silicon oxide layer is naturally formed on the semiconductor layer.

Also, in a method for fabricating the thin film transistor array substrate, a semiconductor layer is formed on an insulating substrate. A gate insulating layer is formed on the substrate such that the gate insulating layer covers the semiconductor layer. A gate line assembly is formed on the gate insulating layer with an Ag alloy. The Ag alloy comprises Ag and at least one of alloy elements and the alloy elements each bear a low melting point. The gate line assembly comprises a gate electrode and a gate line. A source and a drain region are formed through doping the semiconductor layer with impurities and while defining a channel region. An inter-layered insulating layer is formed on the substrate such that the inter-layered insulating layer covers the gate line assembly. Contact holes exposing the source and the drain regions are formed in the inter-layered insulating layer and the gate insulating layer. A data line assembly is formed on the inter-layered insulating layer. The data line assembly comprises a source electrode connected to the source region, a drain electrode connected to the

drain region, and a data line. A protective layer is formed on the substrate such that the protective layer covers the data line assembly. A contact hole exposing the drain electrode is formed in the protective layer. A pixel electrode is formed on the protective layer such that the pixel electrode is connected to the drain electrode through the contact hole.

Herein, the gate line assembly or the data line assembly may be formed with an Ag alloy. The Ag alloy for the line assembly comprises Ag and at least one of alloy elements and the alloy elements each bear a low melting point. The gate line assembly is formed through depositing an Ag alloy layer onto the substrate through sputtering a target of the Ag alloy with an oxygen concentration of 5000ppm or less. The Ag alloy layer is patterned through photolithography.

The protective layer is formed through heat treatment at 200℃ or more. The alloy element of the Ag alloy layer for the data line assembly reacts with a silicon oxide layer to form an alloy element – oxide layer during the process of heat treatment for forming the protective layer where the silicon oxide layer is naturally formed on the semiconductor layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a large-size high resolution liquid crystal display, it is essential to develop a low resistance metal-based wiring line assembly. For this reason, silver (Ag) bearing a lowest resistance among metal has been studied to use for the wiring line assembly.

However, in order to use Ag for the wiring line assembly, suitable processing conditions should have been first developed, considering the material aspects of Ag.

Pure silver exhibits poor adhesion characteristic with respect to glass. And its

material characteristics is easily deteriorated under H_2SO_4, NaCl, or KOH. In order to solve such a problem, alloy elements may be added to Ag.

Fig. 1 is a graph illustrating the adhesion test results with respect to Ag, AgAl, AgMg and Cr. A thin film having a thickness of 1 ㎛ is deposited onto a glass substrate through sputtering, and scratched by a scratch tester to measure the adhesion.

In measuring by the scratch tester, a sample is arranged to be inclined by a predetermined angle, and scratched with a diamond tip to measure acoustic emission thereof. When the sampled thin film is broken up, the waveform of the acoustic emission reaches a peak. At this time, the load functioning as a critical load represents the adhesive value between the thin film and the substrate.

It can be known from the graph that the critical load of Ag is about 20N, and that of AgMg is 25N. Furthermore, AgAl and Cr exhibit no peak at the load of 35N or less. It turns out that under the application of Ag alloy to the wiring line assembly, the adhesion thereof with respect to the underlying substrate can be significantly enhanced.

Table 1 indicates variation in the resistivity pursuant to the annealing of Ag, AgAl, and AgMg.

AgMg exhibits a resistivity close to that of Ag. In the case of AgAl, the resistivity thereof is high because it contains much of the Al content and hence, can be sufficiently reduced through lowering the Al content.

Table 1

Temperature	Ag	AgMg (Mg: 1at%)	AgAl (Al: 5at%)
As-dep	1.8732	2.284	7.54125
200℃	1.7136	2.08	7.356

300℃	1.5624	1.9184	7.146
400℃	1.666	1.9472	6.279
500℃	1.666	1.8784	6.381
600℃	1.666	1.7344	6.426
700℃	11.3008	1.948	7.5

According to Fig. 1 and Table 1, an Ag alloy with alloy content such as Mg and Al at a suitable proportion is used for the wiring line assembly, the adhesion characteristic thereof with respect to the underlying substrate is improved while the resistivity thereof being close to Ag.

Figs. 2, 3, 4 and 5 illustrate the auger electron spectroscopy (AES) analysis data with respect to the layered structure of an Ag alloy-based layer, a silicon oxide layer, and a silicon layer after and before the annealing.

Fig. 2 is a graph illustrating the AES analysis results for a sample of an AgMg-based layer under deposition. Fig. 3 is a graph illustrating the AES analysis results for a sample of an AgMg-based layer that is heat-treated at 400℃ under a vacuum atmosphere. Fig. 4 is a graph illustrating the AES analysis results for a sample of an AgAl-based layer under deposition. Fig. 5 is a graph illustrating the AES analysis results for a sample of an AgAl-based layer that is heat-treated at 400℃ under a vacuum atmosphere.

In the graphs, the sputter etching time at the horizontal axis is established to be 8min before the annealing, and 20min after the annealing. This means that the

measurement is made at the surface of the Ag alloy-based layer before the annealing, and to the interface between the Ag alloy-based layer and a lower layer thereof after the annealing.

AgMg or AgAl is sputtered at 150℃. An oxide layer of MgO or Al_2O_3 is formed on the surface of the Ag alloy-based layer directly after the sputtering.

The Mg or Al element moves to the interface between the Ag alloy-based layer and the silicon oxide layer at 400℃ under the vacuum atmosphere, and reacts with oxygen there while forming MgO or Al_2O_3. Considering that the oxygen content appears to present on the surface of the Ag alloy-based layer even before the annealing, it turns out that the oxygen content is segregated onto the surface of the target layer only with the temperature of deposition.

This result is due to the rapid diffusion speed as well as the surface segregation of the alloy content of Mg or Al. Particularly, Mg appears to be present only on the surface and the interface of the Ag alloy-based layer after the annealing. This means that the surface segregation effect of Mg is great.

Figs. 6A and 6B conceptually illustrate the theoretical background for the above data.

When the AgMg-based layer shown in Fig. 6A is heat-treated under an oxygen atmosphere, as shown in Fig. 6B, the Mg element moves to the layer surface to thereby form an oxide layer of MgO.

Furthermore, the Mg element also moves to the layer interface between the Ag alloy-based layer and the silicon oxide layer, and reacts with SiO_2 to thereby form MgO. This reaction may be expressed by the chemical formula 1.

$$2Mg+SiO_2 \rightarrow 2MgO+Si,\ \Delta H_{298} = -143.7\ (kcal/mol) \quad (1)$$

The alloy content is exhausted at the wiring line so that the wiring line bears lower resistivity close to that of pure Ag.

As described above, an oxide layer of the alloy element is formed at the surface and the interface between the Ag alloy-based layer and the silicon oxide layer. The oxide layer enhances the adhesion between the Ag alloy-based layer and the neighboring layers or the substrate. Particularly, when the underlying layer is based on silicon, such an oxide layer lowers contact resistance between the Ag alloy-based layer and the silicon-based layer, and prevents diffusion of the Ag content of the Ag alloy-based layer to the silicon-based layer. That is, the Ag alloy-based layer can contact the silicon-based layer in a stable manner.

Such a chemical reaction should be made at a low temperature that can be endured by glass. Furthermore, the alloy content of the Ag alloy-based layer should be exhausted so much as to sufficiently lower the resistivity thereof. In this respect, it becomes important to select alloy elements with a high diffusion speed.

Considering that the diffusion speed of the alloy element is closely related to the melting point, the diffusion speed of the alloy element to the surface and the interface of the Ag alloy-based layer is computed., And the melting point thereof is estimated based on the computed diffusion speed. In this way, suitable alloy elements can be determined.

Let's select an alloy element moving through an Ag-based thin film with a thickness of 0.3 ㎛ for ten (10) minutes when the diffusion of the alloy element is made at 250℃.

The characteristic diffusion length can be expressed by the equation 2.

$$\sqrt{(D \times t)} = 0.3\ \mu m \qquad (2)$$

where D indicates the diffusion coefficient, and t indicates the period of time.

It results from the equation 2 that D = 1.5E-12 cm^2/sec. Thus, it is preferable to select an alloy element having such a diffusion coefficient value or more.

Meanwhile, the particle interface diffusion controls the overall diffusion at the temperature lower than 0.5×Tm (Tm refers to the melting point of the alloy element). Thus, the equation 3can be induced.

$$T < 0.5 \times Tm \qquad (3)$$

where T indicates the current temperature, and Tm indicates the melting point of the alloy element.

Furthermore, in the metallic material having a structure of face-centered cubic crystal(FCC), the diffusion coefficient thereof can be obtained by the equation 4.

$$D = 0.3 \times \exp(-8.5 \times Tm/T)\ cm^2/sec \qquad (4)$$

In consideration of such conditions, the available range of melting point and diffusion coefficient for suitable alloy elements can be determined.

Fig. 7 graphically illustrates the equation 4 where T is replaced by 523K (250℃). In the graph, the horizontal axis indicates the melting point Tm, and the vertical axis indicates the diffusion coefficient D.

It can be estimated from the graph that the melting point Tm should be 1500K or less to obtain a diffusion coefficient of 1.5E-12 cm^2/sec or more.

Fig. 8 is a graph illustrating the available range of melting point and enthalpy for suitable alloy elements. In the graph, the alloy elements having a melting point lower

than 1500K and an oxide formation energy greater than that of SiO_2 are exemplified.

As the metallic material bearing a low melting point exhibits lower surface energy, surface segregation thereof is liable to occur in a large scale. In this connection, as shown in Fig. 8, Li, Mg, Al, Sm or Mn is turned out to be a suitable alloy element.

The Ag alloy for the wiring line assembly may be based on a double-sourced alloy, a triple-sourced alloy, or a quadruple-sourced alloy selected from Ag, and Li, Mg, Al, Sm, or Mn.

The composition ratio of the alloy content to the Ag alloy should be 20at% or less in consideration of the resistivity of the Ag alloy. For instance, in the case of a quadruple-sourced alloy of Ag-a-b-c, it is preferable that the content ratio of a, b and c should be established to be $0.1at\% \leq a \leq 20at\%$, $0.1at\% \leq b \leq 20at\%$, $0.1at\% \leq c \leq 20at\%$, and $a+b+c \leq 20at\%$.

As described above, the Ag alloy with an alloy content of Li, Mg, Al, Sm or Mn may be used to form a low resistance wiring line assembly for a wide screen display device. In this case, the wiring line assembly can bear good contact characteristic with the neighboring layers while insuring the interface stability thereof.

Furthermore, it is possible to apply such an Ag alloy-based wiring line assembly for use in a reflection type liquid crystal display.

A thin film transistor array substrate with an Ag alloy-based wiring line assembly and a method for fabricating the same will be now explained with reference to the drawings.

Fig. 9 is a plan view of a thin film transistor array substrate according to a first preferred embodiment of the present invention, and Fig. 10 is a cross sectional view of

the thin film transistor array substrate taken along the X-X' line of Fig. 9.

A gate line assembly is formed on an insulating substrate 10 with a silver (Ag) alloy bearing a low resistance. The gate line assembly includes a gate line 22 proceeding in the horizontal direction, a gate pad 24 connected to end of the gate line 22 to receive gate signals from the outside and transmit them to the gate line 22, and a gate electrode 26 for TFT connected to the gate line 22.

The Ag alloy for the gate line assembly is formed with a main content of Ag and an alloy content of metallic elements bearing a high diffusion coefficient and a low melting point. The alloy content may be selected from Li, Mg, Al, Sm, or Mn. It is preferable that the metallic elements for the alloy content bear a diffusion coefficient of 1.5E-12 cm^2/sec or more, and a melting point of 1500K or less.

One, two or three metallic elements may be used for the alloy content. That is, the Ag alloy for the gate line assembly may be a double-sourced alloy, a triple-sourced alloy, or a quadruple-sourced alloy. It is preferable that the composition ratio of the alloy content to the Ag alloy should be 10at% or less.

As the Ag alloy exhibits good adhesion characteristic with respect to glass, the gate line assembly tightly adheres to the substrate 10 without getting loose.

A gate insulating layer 30 is formed on the substrate 10 with silicon nitride to cover the gate line assembly.

An island-shaped semiconductor pattern 40 is formed on the gate insulating layer 30 over the gate electrode 24 with hydrogenated amorphous silicon. Ohmic contact patterns 55 and 56 are formed on the semiconductor pattern 40 with hydrogenated amorphous silicon where n-type impurities are doped at high

concentration.

A metallic oxide layer 510 is formed on the ohmic contact patterns 55 and 56. The metallic oxide layer 510 may be formed of MgO, Al_2O_3, or Li_2O depending upon the material for a data line assembly to be described later. In case AgMg or AgAl is used for the data line assembly, the metallic oxide layer 510 is formed with MgO, or Al_2O_3.

The aforementioned data line assembly is formed on the metallic oxide layer 510 and the gate insulating layer 30 with an Ag alloy bearing a low resistance.

As like in the case of the gate line assembly, the Ag alloy for the data line assembly is formed with a main content of Ag, and an alloy content of metallic elements bearing a high diffusion coefficient and a low melting point. The alloy content may be selected from Li, Mg, Al, Sm, or Mn.

The data line assembly includes a data line 62 proceeding in the vertical direction while crossing over the gate line 22, a source electrode 65 branched from the data line 62 while being extended over the metallic oxide layer 510 on the one-sided ohmic contact pattern 55, a data pad 68 connected to the one-sided end of the data line 62 to receive picture signals from the outside, and a drain electrode 66 formed on the other-sided ohmic contact pattern 56 around the gate electrode 26 while being separated from the source electrode 65.

In this structure, the metallic oxide layer 510 is disposed between the Ag alloy-based layer for the data line assembly and the silicon-based layer for the ohmic contact patterns 55 and 56. The metallic oxide layer 510 lowers the contact resistance between the two neighboring layers while enhancing the adhesion thereof, and prevents diffusion of the Ag content of the Ag alloy-based layer to the silicon-based layer.

A protective layer 70 is formed on the data line assembly with silicon nitride.

Contact holes 76 and 78 exposing the drain electrode 66 and the data pad 68 are formed at the protective layer 70, and a contact hole 74 exposing the gate pad 24 together with the gate insulating layer 30 are also formed in the protective layer 70.

A pixel electrode 82 is formed on the protective layer 70 such that it is electrically connected to the drain electrode 66 through the contact hole 76. Furthermore, a subsidiary gate and a subsidiary data pads 86 and 88 are formed on the protective layer 70 such that they are connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78. The pixel electrode 82, and the subsidiary gate and data pads 86 and 88 are formed with indium tin oxide (ITO) or indium zinc oxide (IZO).

A method for fabricating the thin film transistor array substrate will be now explained with reference to Figs. 11A to 15B, and Figs. 9 to 10.

As shown in Figs. 11A and 11B, an Ag alloy-based layer is deposited onto a substrate 10, and patterned to thereby form a gate line assembly. The Ag alloy for the gate line assembly is formed with a main content of Ag, and an alloy content of metallic elements bearing a high diffusion coefficient and a low melting point.

The gate line assembly based on the Ag alloy can bear a low resistance characteristic, and a good adhesion characteristic to the glass substrate.

The temperature in fabricating a liquid crystal display is relatively low. This requires that the diffusion coefficient of the alloy element should be high. Therefore, the amount of oxygen in the Ag alloy-based layer should be reduced not to oxidize the highly oxidative alloy element. When the alloy element is oxidized in the Ag alloy-based

layer, the diffusion speed of the alloy element is significantly reduced limiting the above-described effects. Therefore, in the process of depositing the Ag alloy-based layer for the gate line assembly, the oxygen in the Ag alloy target should be limited to 5000ppm or less. Furthermore, the carbon and nitrogen should be also limited to 5000ppm or less.

A metallic oxide layer (not shown) may be formed on the gate line assembly through heat treatment at 200℃ or more under an oxygen atmosphere. In case the gate line assembly is formed of AgMg, an oxide layer of MgO is formed at the interface thereof. In case the gate line assembly is formed of AgAl, an oxide layer of Al_2O_3 is formed at the interface thereof. In these cases, the alloy elements are diffused to the surface and the interface of the gate line assembly through the heat treatment. This reduces the resistivity of the gate line assembly, and enhances its adhesion to the substrate.

The gate line assembly may be naturally heat-treated at the subsequent process of depositing an insulating layer without requiring any separate process.

Thereafter, as shown in Figs. 12A and 12B, a silicon nitride-based gate insulating layer 30, a hydrogenated amorphous silicon-based layer 40, and an impurities-doped hydrogenated amorphous silicon-based layer 50 are sequentially deposited onto the substrate 10. The hydrogenated amorphous silicon-based layer 40, and the impurities-doped hydrogenated amorphous silicon-based layer 50 are patterned through photolithography to thereby form an island-shaped semiconductor pattern 40 and an island-shaped ohmic contact pattern 50 on the gate insulating layer 30 over the gate electrode 24.

As shown in Figs. 13A and 13B, an Ag alloy-based layer is deposited onto the ohmic contact pattern 50 and the gate insulating layer 30, and patterned through photolithography to thereby form a data line assembly. The Ag alloy for the data line assembly is formed with a main content of Ag, and an alloy content of metallic elements bearing a high diffusion coefficient and a low melting point.

The data line assembly includes a data line 62 crossing over the gate line 22, a source electrode 65 connected to the data line 62 while being extended over the gate electrode 26, a data pad 68 connected to one-sided end of the data line 62, and a drain electrode 66 separated from the source electrode 65 while facing the source electrode 65 around the gate electrode 26.

Thereafter, the ohmic contact pattern 50 exposed through the source and the drain electrodes 65 and 66 is etched such that it is divided into an ohmic contact pattern 55 contacting the source electrode 65, and an ohmic contact pattern 56 contacting the drain electrode 66.

As shown in Figs. 14A and 14B, a protective layer 70 is deposited onto the substrate 10 with an inorganic insulating material such as silicon nitride. It is preferable that the protective layer 70 should be deposited at the temperature range of 200℃ or more.

In the process of forming the protective layer 70, a metallic oxide layer 510 may be formed between the Ag alloy-based layer for the source and drain electrodes 65 and 66, and the silicon-based layers for the ohmic contact patterns 55 and 56 and the semiconductor pattern 40.

The metallic oxide layer 510 is based on a silicon oxide layer that is naturally

formed on the silicon-based layers before forming the Ag alloy-based layer for the data line assembly.

The alloy elements of the Ag alloy-based layer are diffused to the interface while making the silicon oxide layer to be a dense-structured metallic oxide layer 510. In case the data line assembly is based on AgMg, MgO is formed at the interface thereof. In case the data line assembly is based on AgAl, Al_2O_3 is formed at the interface thereof.

The metallic oxide layer 510 lowers the contact resistance between the data line assembly and the silicon-based patterns 40, 55 and 56 while enhancing the adhesion therebetween. This serves to obtain a stable interface characteristic of the data line assembly. Furthermore, the alloy element is exhausted from the data line assembly so that the material content for the data line assembly bears a pure Ag characteristic, which reduces the resistivity.

In the usual case, surface of the silicon-based layers 40 and 50 is rinsed using HF before the formation of the data line assembly. However, even without the rinsing process using HF, the contact characteristic between the source and the drain electrodes 65 and 66 and the semiconductor pattern 40 as well as the ohmic contact patterns 55 and 56 can be improved by way of the interposed metallic oxide layer. Alternatively, in order to obtain such effects, a silicon oxide layer with 30Å or less may be deposited onto the silicon-based layers through chemical vapor deposition (CVD).

Thereafter, as shown in Figs. 15A and 15B, the protective layer 70 is patterned together with the gate insulating layer 30 through photolithography to thereby form contact holes 74, 76 and 78 exposing the gate pad 24, the drain electrode 66, and the

data pad 68.

An ITO or IZO-based layer is deposited onto the protective layer 70, and patterned through photolithography to thereby form a pixel electrode 82 connected to the drain electrode 66 through the contact hole 76, and a subsidiary gate and a subsidiary data pads 86 and 88 connected to the gate and the data pads 24 and 68 through the contact holes 74 and 78.

In the above-structured thin film transistor array substrate, the gate line assembly and the data line assembly are formed with an Ag alloy bearing a low resistance so that they can be well adapted for use in a wide-screened high definition liquid crystal display. Furthermore, they can reduce the contact resistance between the neighboring layers and can improve the adhesion therebetween.

The above structure can be applied to a thin film transistor array substrate using poly-crystalline silicon thin film transistors.

Fig. 16 is a plan view of a thin film transistor array substrate according to a second preferred embodiment of the present invention. Fig. 17 is a cross sectional view of the thin film transistor array substrate taken along the XVII-XVII' line of Fig. 16.

An island-shaped semiconductor pattern 121 is formed on an insulating substrate 100 with poly-crystalline silicon. The semiconductor pattern 121 is formed with a channel region 122, a source and a drain regions 125 and 126 with high concentration impurities, and LDD regions with low concentration impurities placed between the channel and the source regions 122 and 125, and between the channel and the drain regions 122 and 126.

The LDD regions 123 and 124 are resistors that minimize leakage of current at

an OFF state of the thin film transistor with a poly-crystalline semiconductor channel and components.

A gate insulating layer 130 is formed on the insulating substrate 100 while covering the semiconductor pattern 121.

A gate line assembly is formed on the gate insulating layer 130 with an Ag alloy. The Ag alloy for the gate line assembly is formed of a main content of Ag, and an alloy content of metallic materials bearing a high diffusion coefficient and a low melting point. The gate line assembly includes a gate line 141, a gate pad 142 connected to end of the gate line 141 to receive gate signals from the outside and transmit them to the gate line 141, and a gate electrode 143 connected to the gate line 141 corresponding to the channel region 122 of the semiconductor pattern 121.

As described above, if the gate line assembly is formed of an Ag alloy, it can bear a low resistance characteristic, and a stable interface characteristic.

An inter-layer insulating layer 150 based on silicon nitride covers the gate line assembly.

The inter-layer insulating layer 150 and the gate insulating layer 130 are provided with a contact hole 161 exposing the source region 125, and a contact hole 162 exposing the drain region 126.

A data line assembly is formed on the inter-layer insulating layer 150 with an Ag alloy. The Ag alloy for the data line assembly is formed with a main content of Ag, and an alloy content of metallic materials bearing a high diffusion coefficient and a low melting point. The data line assembly includes a data line 171 crossing over the gate line 141, a data pad 172 extended from end of the data line 171, a source electrode 173

protruded from the data line 171 while contacting the source region 125 of the semiconductor pattern 121, and a drain electrode 174 contacting the drain region 126 of the semiconductor pattern 121 while facing the source electrode 173.

A metallic oxide layer 510 is formed between the source electrode 173 and the source region 125 of the semiconductor pattern 121, and between the drain electrode 174 and the drain region 126 of the semiconductor pattern 121.

The metallic oxide layer 510 may be formed of MgO, Al_2O_3, or Li_2O depending upon the material for the data line assembly. If the data line assembly is based on AgMg or AgAl, a metallic oxide layer would be MgO or Al_2O_3.

The metallic oxide layer 510 is formed between the Ag alloy-based layer for the source and the drain electrodes 173 and 174 and the silicon-based layer for the semiconductor pattern 121 to lower the contact resistance between the two layers while enhancing the adhesion therebetween. Furthermore, the metallic oxide layer 510 provides a cleaner interface that prevents the Ag element of the Ag alloy-based layer from diffusing into the silicon-based layer.

A protective layer 180 is formed of silicon nitride to cover the data line assembly.

The protective layer 180 is provided with contact holes 191 and 192 exposing the drain electrode 174 and the data pad 172, and a contact hole 193 exposing the gate pad 142 together with the inter-layer insulating layer 150.

A pixel electrode 201 is formed on the protective layer 180 such that is electrically connected to the drain electrode 174 through the contact hole 191. Furthermore, a subsidiary data and subsidiary gate pads 202 and 203 are formed on the protective layer 180 such that they are connected to the data and gate pads 172

and 142 through the contact holes 192 and 193. The pixel electrode 201, and the subsidiary data and gate pads 202 and 203 are formed of ITO or IZO.

A method for fabricating the thin film transistor array substrate will be now explained with reference to Figs. 18A through 22B.

As shown in Figs. 18A and 18B, a poly-crystalline silicon-based layer is formed on an insulating substrate 100, and patterned through photolithography to form an island-shaped semiconductor pattern 121.

The poly-crystalline silicon layer may be formed through depositing an amorphous silicon-based layer onto the substrate, and crystallizing the amorphous silicon by way of a silicon crystallization technique such as laser annealing, or high temperature solidification.

Thereafter, as shown in Figs. 19A and 19B, a gate insulating layer 130 is formed on the substrate 100 such that it covers the semiconductor pattern 121. An Ag alloy-based layer is deposited onto the gate insulating layer 130, and patterned to thereby form a gate line assembly. The Ag alloy for the gate line assembly is formed with a main content of Ag, and an alloy content of metallic elements having a high diffusion coefficient and a low melting point. The gate line assembly includes a gate line 141, a gate pad 142, and a gate electrode 143.

As shown in Figs. 20A and 20B, a source and a drain regions 125 and 126 with high concentration impurities, and LDD regions 123 and 124 with low concentration impurities are formed at the semiconductor pattern 121. The portion of the semiconductor pattern 121 overlapped by the gate electrode 143 and not doped with impurities becomes a channel region 122.

In order to form such impurity-doped regions 123, 124, 125 and 126 in the semiconductor pattern 121, the semiconductor pattern 121 except for the channel portion is doped with n-type impurities at low concentration while using the gate electrode 143 as a mask. Then, covering with a doping mask the gate electrode 143, the channel region 122 and the LDD regions 123 and 124 of the semiconductor pattern 121 are doped with n-type impurities at high concentration through the doping mask to dope the periphery of the semiconductor pattern 121 not blocked by the doping mask at high concentration.

At this time, the periphery of the semiconductor pattern 121 doped at low concentration and re-doped at high concentration becomes to be the source and the drain regions 125 and 126 with high concentration impurities., The portions of the semiconductor pattern 121 doped at low concentration becomes the LDD regions 123 and 124 with low concentration impurities, and the portions of the semiconductor pattern 121 that is not doped becomes the channel region 122.

The order of low concentration doping process and the high concentration doping process may be reversed.

Thereafter, as shown in Figs. 21A and 21B, an inter-layered insulating layer 150 is formed on the entire surface of the substrate 100 while covering the gate line

assembly. The inter-layered insulating layer 150 and the gate insulating layer 130 are patterned through photolithography to thereby form a contact hole 161 exposing the source region 125, and a contact hole 162 exposing the drain region 126.

An Ag alloy-based layer is then deposited onto the inter-layered insulating layer 150, and patterned to thereby form a data line assembly. The Ag alloy for the data line assembly is formed with a main content of Ag, and an alloy content of metallic elements having a high diffusion coefficient and a low melting point. The data line assembly includes a data line 171 crossing over the gate line 141, a source electrode 173 connected to the data line 171 while contacting the source region 125 through the contact hole 161, a data pad 172 connected to one end of the data line 141, and a drain electrode 174 separated from the source electrode 173 while contacting the drain region 126 through the contact hole 162.

Thereafter, as shown in Figs. 22A and 22B, a protective layer 180 is deposited onto the substrate 100 with an inorganic insulating material such as silicon nitride. It is preferable that the protective layer 180 is deposited at the temperature range of 200℃ or more.

In the heat treatment process for forming the protective layer 180, a metallic oxide layer 510 may be formed between the source electrode 173 and the semiconductor pattern 121, and between the drain electrode 174 and the semiconductor pattern 121. The metallic oxide layer 510 is formed due to a silicon oxide layer naturally formed on the semiconductor pattern before forming the Ag alloy-based layer for the data line assembly.

In the heat treatment process for forming the protective layer 180, the alloy

elements of the Ag alloy-based layer for the data line assembly is diffused to the interface and make the silicon oxide layer to be a dense-structured metallic oxide layer 520. If the data line assembly is based on AgMg, a metallic oxide layer of MgO is formed at the interface. If the data line assembly is based on AgAl, a metallic oxide layer of Al_2O_3 is formed at the interface.

The metallic oxide layer 510 lowers the contact resistance between the data line assembly and the semiconductor pattern 121 and enhances the adhesion therebetween.

Thereafter, as shown in Figs. 23A and 23B, the protective layer 180 is patterned through photolithography to thereby form a contact hole 191 exposing the drain electrode 174, and a contact hole 192 exposing the data pad 172. Furthermore, the protective layer 180 is patterned together with the inter-layer insulating layer 150 to thereby form contact holes 193 exposing the gate pads 142.

Finally, an ITO or IZO-based layer is deposited onto the protective layer 180, and patterned through a mask to thereby form a pixel electrode connected to the drain electrode 174 through the contact hole 191, and a subsidiary data and a subsidiary gate pads 202 and 203 connected to the data and the gate pads 172 and 142 through the contact holes 192 and 193.

In the thin film transistor array substrate according to the second preferred embodiment of the present invention, the gate line assembly and the data line assembly are formed with an Ag alloy bearing a low resistance. Consequently, such a thin film transistor array substrate can be well adapted for use in a wide-screen high definition liquid crystal display. Furthermore, the contact resistance between the neighboring layers can be reduced.

As described above, in the inventive thin film transistor array substrate, the target wiring lines are formed with an Ag alloy bearing a low resistance. Such a thin film transistor array substrate can be well adapted for use in a wide-screen high definition display device. Furthermore, the contact resistance between the neighboring lines can be reduced while giving reliability to the resulting display device.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A wiring line assembly for a display device, comprising:

a wire formed of an Ag alloy,

wherein the Ag alloy includes Ag and an alloy element bearing a low melting point and high diffusion coefficient.

2. The wiring line assembly of claim 1, wherein the alloy element bears a diffusion coefficient of 1.5E-12 cm^2/sec or more.

3. The wiring line assembly of claim 1, wherein the alloy element bears a melting point of 1500K or less.

4. The wiring line assembly of claim 1, wherein the composition content of the alloy element is 10at% or less.

5. The wiring line assembly of claim 1, wherein the alloy element is selected from the group consisting of Li, Mg, Al, Sm, and Mn.

6. The wiring line assembly of claim 1, wherein the Ag alloy is used for reflection electrodes for a reflection type liquid crystal display.

7. A thin film transistor array substrate, comprising:

a gate line assembly made of an Ag alloy, the gate line assembly including a gate electrode and a gate line;

a data line assembly crossing over the gate line assembly while being insulated from the gate line assembly, the data line assembly including a source electrode, a drain electrode and a data line;

a semiconductor layer contacting the source electrode and the drain electrode, the semiconductor layer forming a thin film transistor together with the gate electrode, the source electrode and the drain electrode; and

a pixel electrode connected to the drain electrode,

wherein the Ag alloy comprises Ag and an alloy element bearing a low melting point and high diffusion coefficient.

8. The thin film transistor array substrate of claim 7, wherein the data line assembly is also made of the Ag alloy, wherein the Ag alloy comprises Ag and an alloy element bearing a low melting point and high diffusion coefficient.

9. The thin film transistor array substrate of claim 7 or claim 8, wherein the alloy element bears a diffusion coefficient of 1.5E-12 cm^2/sec or more.

10. The thin film transistor array substrate of claim 7 or claim 8, wherein the alloy element bears a melting point of 1500K or less.

11. The thin film transistor array substrate of claim 7 or claim 8, wherein the composition content of the alloy element is 10at% or less.

12. The thin film transistor array substrate of claim 7 or claim 8, wherein the alloy element is selected from the group consisting of Li, Mg, Al, Sm, and Mn.

13. The thin film transistor array substrate of claim 7, further comprising:

an insulating substrate under the gate line assembly;

a gate insulating layer covering the gate line assembly and being under the semiconductor layer; and

a protective layer covering the data line assembly with a contact hole exposing the drain electrode,

wherein the drain electrode is placed on the semiconductor layer together with the source electrode and the pixel electrode is connected to the drain electrode through the contact hole.

14. The thin film transistor array substrate of claim 13, wherein the semiconductor layer is formed of hydrogenated amorphous silicon.

15. The thin film transistor array substrate of claim 13, further comprising an oxide layer formed on the gate line assembly.

16. The thin film transistor array substrate of claim 13, further comprising an alloy element - oxide layer interposed between the source electrode and the semiconductor layer and between the drain electrode and the semiconductor layer.

17. The thin film transistor array substrate of claim 7, further comprising:

an insulating substrate under the semiconductor layer, the semiconductor layer comprising a source region, a drain region and a channel region;

a gate insulating layer covering the semiconductor layer and being under the gate line assembly;

an inter-layer insulating layer covering the gate line assembly, the inter-layer insulating layer and the gate insulating layer having contact holes exposing the source region and the drain region, the source electrode and the drain electrode being respectively connected to the source region and the drain region through the contact holes; and

a protective layer covering the data line assembly with a contact hole exposing the drain electrode, the pixel electrode being connected to the drain electrode through the contact hole of the protective layer.

18. The thin film transistor array substrate of claim 17, wherein the semiconductor layer is formed of poly-crystalline silicon.

19. The thin film transistor array substrate of claim 17, further comprising an alloy element - oxide layer interposed between the source electrode and the semiconductor layer and between the drain electrode and the semiconductor layer.

20. A method for fabricating a thin film transistor array substrate, comprising the steps of:

forming a gate line assembly on an insulating substrate with an Ag alloy, the Ag alloy comprising Ag and an alloy element bearing a low melting point and high diffusion coefficient, the gate line assembly comprising a gate electrode and a gate line;

forming a gate insulating layer on the substrate such that the gate insulating layer covers the gate line assembly;

forming a semiconductor layer on the gate insulating layer;

forming a data line assembly on the semiconductor layer, the data line assembly comprising a source electrode, a drain electrode and a data line;

forming a protective layer on the substrate such that the protective layer covers the data line assembly;

forming a contact hole exposing the drain electrode at the protective layer; and

forming a pixel electrode on the protective layer such that the pixel electrode is

connected to the drain electrode through the contact hole.

21. The method of claim 20 wherein the data line assembly is formed of the Ag alloy, the Ag alloy comprising Ag and an alloy element bearing a low melting point and high diffusion coefficient.

22. The method of claim 20 or claim 21, wherein the gate line assembly is formed through depositing the Ag alloy layer onto the substrate through sputtering a target of the Ag alloy with an oxygen concentration of 5000ppm or less, and patterning the Ag alloy layer through photolithography.

23. The method of claim 20, wherein the protective layer is formed through heat treatment at 200℃ or more.

24. The method of claim 23, wherein the alloy element of the Ag alloy layer for the data line assembly reacts with a silicon oxide layer to form an alloy element – oxide layer during the process of heat treatment for forming the protective layer and the silicon oxide layer is naturally formed on the semiconductor layer.

25. A method for fabricating a thin film transistor array substrate, comprising the steps of:

forming a semiconductor layer on an insulating substrate;

forming a gate insulating layer on the substrate such that the gate insulating layer covers the semiconductor layer;

forming a gate line assembly on the gate insulating layer with an Ag alloy, the Ag alloy comprising Ag and an alloy element bearing a low melting point, the gate line

assembly comprising a gate electrode and a gate line;

forming a source region and a drain region through doping the semiconductor layer with impurities while defining a channel region;

forming an inter-layer insulating layer on the substrate to cover the gate line assembly;

forming contact holes exposing the source and the drain regions in the inter-layer insulating layer and the gate insulating layer;

forming a data line assembly on the inter-layer insulating layer, the data line assembly comprising a source electrode connected to the source region, a drain electrode connected to the drain region, and a data line;

forming a protective layer on the substrate to cover the data line assembly;

forming a contact hole exposing the drain electrode in the protective layer; and

forming a pixel electrode on the protective layer such that the pixel electrode is connected to the drain electrode through the contact hole.

26. The method of claim 25, wherein the data line assembly is formed of the Ag alloy, the Ag alloy comprising Ag and an alloy element bearing a low melting point and high diffusion coefficient.

27. The method of claim 25 or claim 26, wherein the gate line assembly is formed through depositing the Ag alloy layer onto the substrate through sputtering a target of the Ag alloy with an oxygen concentration of 5000ppm or less, and patterning the Ag alloy layer through photolithography.

28. The method of claim 25, wherein the protective layer is formed through heat treatment at 200℃ or more.

29. The method of claim 28, wherein the alloy element of the Ag alloy layer for the data line assembly reacts with a silicon oxide layer to form an alloy element – oxide layer during the process of heat treatment for forming the protective layer and the silicon oxide layer is naturally formed on the semiconductor layer.